ABSTRACT OF THE DISCLOSURE

A core logic chipset for a computer system is provided which can be configured as a

bridge between either an accelerated graphics port (AGP) bus or an additional peripheral

component interconnect (PCI) bus. A common bus having provisions for the PCI and AGP

5   interface signals is connected to the core logic chipset and either an AGP or PCI device(s). The

common bus, which is part of a fault-tolerant interconnect system, includes a first bus portion

and a lower bus portion. When an error (e.g., a parity error) is detected on the first bus portion,

the transaction is transferred over the second bus portion. When an error is detected on the

second bus portion, the transaction is transferred over the first bus portion. If errors are detected

10   on both portions, the transaction may be terminated.